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LEFKOWITZ, SUMATI	
ART UNIT	**PAPER NUMBER**
2112	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/033,142	Applicant(s) GULICK, DALE E.	
	Examiner Sumati Lefkowitz	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *19-23,30 and 31* is/are withdrawn from consideration.

5)☒ Claim(s) *40-47* is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-25,27-33 and 35-38* is/are rejected.

7)☒ Claim(s) *4,10,26,34 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 5*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *6*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18, 24-29, and 32-47 are pending. Claims 19-23 and 30-31 are being withdrawn as being directed to a non-elected invention.

Specification

2. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-18, 24-29, 32-47, drawn to exchanging data between an Ethernet controller and a microcontroller over an internal bus, classified in class 710, subclass 305.

II. Claims 19-23 and 30-31, drawn to a microcontroller connected to an internal bus and configured to write a system management interrupt vector to a system management interrupt request register, classified in class 710, subclass 260.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as

in systems that do not have a microcontroller that is configured to write a system management interrupt vector to a system management interrupt request register. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mark W. Sincell (#52,226) on June 9, 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-18, 24-29, and 32-47. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19-23 and 30-31 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6, 7, 11, 24, 25, 27, 33, rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay et al., 2002/0194415 A1 (hereinafter Lindsay).

a. As to claims 1-3, 6, 7, 11, 24, 25, 27, 33, Lindsay discloses an integrated circuit (note abstract and Figures 7 and 8), comprising: an internal bus (note Figure 8, 811); a microcontroller (note Figure 8, 825) connected to the internal bus, wherein the microcontroller is configured to master the internal bus (i.e., inherent); an Ethernet controller (note Figure 8, 808) coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus; and a plurality of buffers (note Figure 8, 818 and buffers included within MAC 808) coupled between the microcontroller and the Ethernet controller for buffering the data, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller, wherein the microcontroller (i.e., alert supervisory bus controller) is configured as an Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller (note Figures 7 and 8, abstract, [0083-0085]), further comprising: a status register configured to store Alert Standard Format sensor data, wherein the Alert Standard Format sensor data is stored in the status register by the microcontroller (note Figure 7, 724 and Figure 8, 824), further comprising: a power port configured to receive a reserve power signal, wherein the reserve power signal provides reserve power to the status register configured to store Alert Standard Format sensor data (i.e., inherent to ASF, ACPI – [0075]), further comprising: a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured (note [0080]).

b. As to claims 12-16, Lindsay discloses that the integrated circuit further comprises a memory connected to the internal bus, wherein the memory includes a read-only memory, wherein the memory includes random access memory, wherein the random access memory is configured to shadow a read-only memory, wherein the random access memory is loaded during a boot-up process (note Figure 9, [0101]).

c. As to claims 17, 18, 28, 29, 37, and 38, Lindsay discloses that the microcontroller is configured to manage security in a computer system and the microcontroller is configured to manage health status of a computer system (note [0074, 0076]).

d. As to claim 32, the claimed elements have already been discussed with respect to claim 1 above, with the exception of an external bus and a processor coupled to the external bus, wherein the processor is configured to communicate over a network using the Ethernet controller.

Lindsay discloses an external bus (note Figures 7, bus 702 and Figure 8, bus 802) and a processor (i.e., inherent to computer system) coupled to the external bus, wherein the processor is configured to communicate over a network using the Ethernet controller.

e. As to claims 35 and 36, the claimed elements have already been discussed with respect to claims 1 and 32 above, with the exception of a computer system comprising bus interface logic coupled to the external bus and one or more sensors coupled to the external bus, wherein the Ethernet controller is configured to transmit data from the sensors over a network or that the microcontroller is configured to poll the sensors over the network.

Lindsay discloses that the computer system comprises bus interface logic (i.e., inherent to communicate over bus) coupled to the external bus and one or more sensors (note Figure 10, sensors 1040, 1050, 1045) coupled to the external bus, wherein the Ethernet controller (note Figure 10, 1020) is configured to transmit data from the sensors over a network (note Figure 10, 1015) and that the microcontroller is configured to poll the sensors over the network (note Figure 10 and [0107]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay et al., 2002/0194415 A1 (hereinafter Lindsay) in view of what was well known in the art, as exemplified by any one of Hwang 6,516,398 and Ma et al., 6,182,235 (hereinafter Ma) and Dea et al., 5,742,833 (hereinafter Dea).

Lindsay fails to disclose that the microcontroller is further configured as an embedded 8051 microcontroller.

Examiner takes Official Notice that embedded 8051 microcontrollers are well known in the art for controlling a variety of devices, including appliances and computer devices, which include NICs, evidence of which may be found in:

Hwang at column 1, lines 27-44

Ma at column 1, lines 11-31

Dea at column 4, lines 1-14.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of an embedded 8051 microcontroller in the system of Lindsay so as to take advantage of its widely recognized small size, low power consumption and versatility.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay et al., 2002/0194415 A1 (hereinafter Lindsay) in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claims 8 and 9, Lindsay fails to disclose that the integrated circuit is configured as a bridge, wherein the bridge further includes: a first bus interface logic for coupling to a first external bus; and a second bus interface logic for coupling to a second external bus.

AAPA discloses that the integrated circuit is configured as a bridge (note Figure 1A, south bridge 112), wherein the bridge further includes: a first bus interface logic for coupling to a first external bus (note Figure 1A, IDE bus 114); and a second bus interface logic for coupling to a second external bus (note Figure 1A, USB 116), wherein the bridge is configured as a south bridge (note Figure 1A, south bridge 112).

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the integrated circuit of Lindsay as a south bridge, as AAPA teaches, so as to allow for the expansion of the system of Lindsay through the use of the bridge to allow for the addition of devices of various protocols to the system of Lindsay.

Allowable Subject Matter

9. Claims 40-47 are allowed.

10. Claims 4, 10, 26, 34, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests systems employing the ASF protocol.

US PG-PUBS: 2003/0028633 A1 Lindsay et al.

2002/0014517 A1 Lindsay et al.

2002/0188875 A1 Hwang et al.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7238 for After-Final communications

703-872-9306 for Official communications

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Sumati Lefkowitz
Primary Examiner
Art Unit 2112

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June 28, 2004